

A New HP-IL to Serial Translator Solution

Application to USB and RS232 PIL-Boxes

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1. Introduction

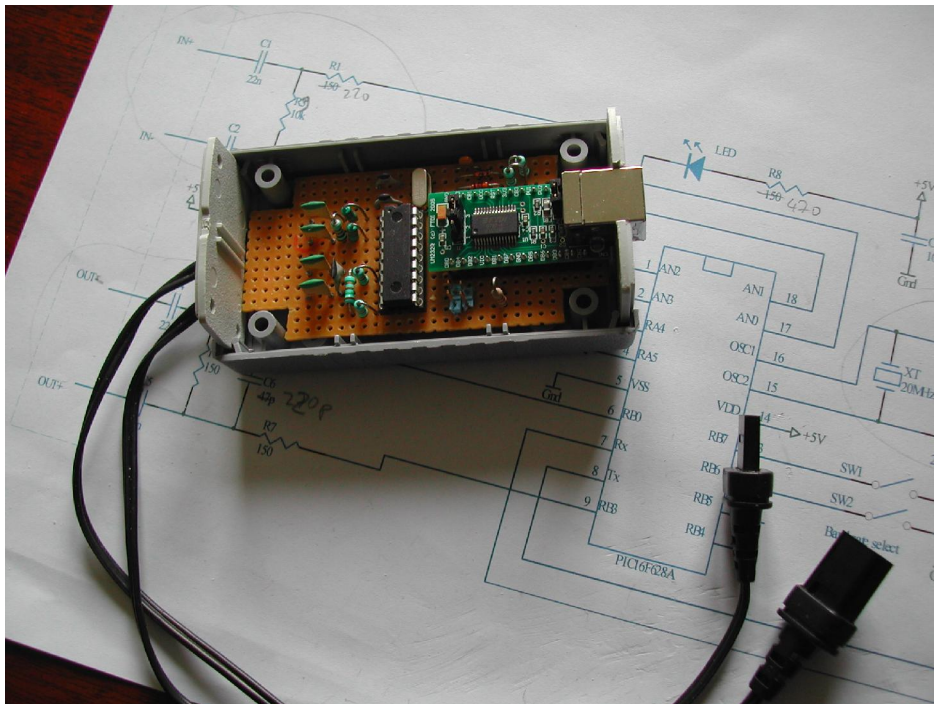
This document describes a HP-IL to serial (TTL level) translator than can be used as the basis of HP-IL/USB and HP-IL/RS232 converters (called here "PIL-Box"). **It uses no obsolete components** such as the HP-IL 1LB3/1LR4 circuits or the specific pulse transformer that were used in the classic HP implementations.

A translator is more than just a HP-IL/serial interface, a HP-IL translator is able to transmit the complete HP-IL protocol from one side to the other of the translator (HP-IL β > serial), not only data as with the classic HP-IL/RS232 HP82164 interface.

The term "translator" was chosen in a reference to the translator mode of the HP-IB/HP-IL HP82169 interface. Similarly the HP-IL/serial translator allows to control HP-IL devices from a computer connected on the serial link side, as well as accessing the computer resources from a HP-IL controller on the loop.

In just a few words, the translator can do everything that could be done with the HP-IL/PC ISA board (HP82973A) in old PCs, but is compatible with virtually any computer or operating system.

The hardware and software aspects are described below and should allow any serious electronic hobbyist to design HP-IL applications for use with the classical HP-41C, HP-71B or HP-75C calculator/computers.



First prototype of an USB PIL-Box.

2. HP-IL description brief summary

The HP-IL connects various devices in a loop, each device receives frames from a two-wire input, and transmits them (after processing) on a separate two-wire output.

HP-IL frames are made of 11 bits: C C C D D D D D D D D.

The first 3 bits are control bits that code the frame type:

C C C

0 E S: DOE: Data (E=0) or End (E=1) bytes, with or without Service Request

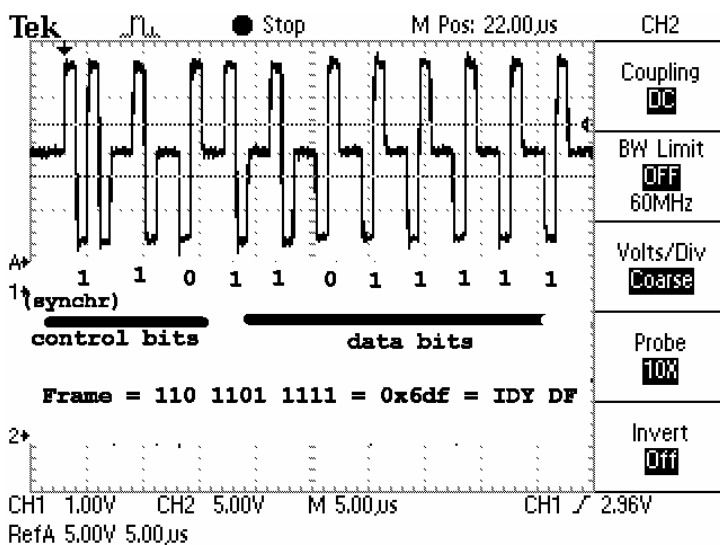
1 0 0: CMD: Command frames

1 0 1: RDY: Ready frames

1 1 S: IDY: Identify frames, with or without Service Request

Physical level:

At the physical level, each bit is transmitted as a positive then negative pulse ('1' bit) or negative then positive pulse ('0' bit). The first control bit is also a synchronisation bit that is twice a normal bit without gap.



Example of the IDY frames automatically sent by a HP-41C when a printer is found or in MANIO mode.

For more details about the HP-IL, please refer to the "HP-IL interface Specification", 82166-90017, november 1982, that gives all the information on the functional, electrical and mechanical aspects of the HP-IL.

3. HP-IL transmitter/receiver hardware implementation

3.1 General

As mentioned above, the goal was to design a system able to manage the HP-IL bus without the specific obsolete components, but using modern ICs that can be easily found.

Several solutions are possible, the choice of the author was to use the minimum of logic and rely as much as possible to microprogramming

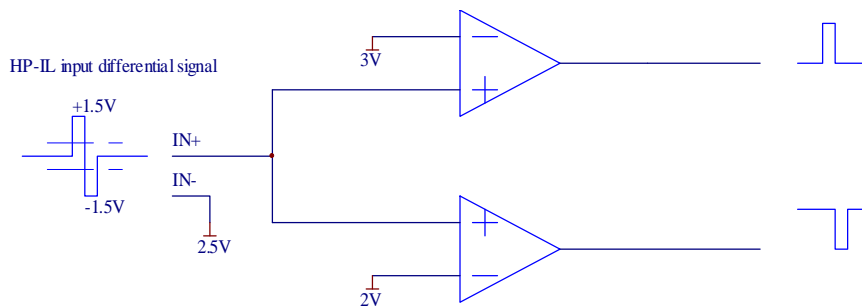
At the physical level, the most difficult task is to receive the HP-IL frame that is using a quite specific coding scheme that is not supported nor trivial to implement on standard uC.

After some thoughts, the following principle was adopted:

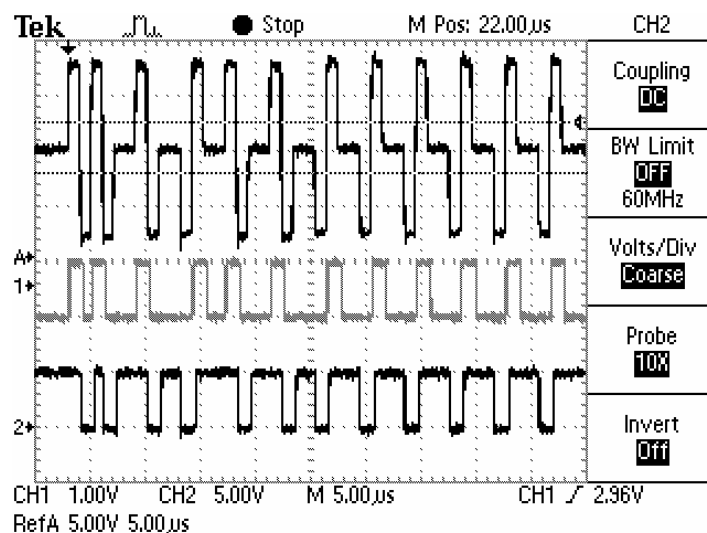
- an analogue receiver will convert the input HP-IL signal into a pair of convenient standard digital signals,
- a PIC microcontroller will sample the digital signals, extract and decode the incoming HP-IL frame, and manage the HP-IL protocol,
- the output HP-IL signal will be driven by the uC with a simple passive analogue matching network.

3.2 HP-IL receiver

The receiver is made of two comparators. The common mode voltage is shifted to 2.5 V. One comparator detects the positive pulses, the other one detects the negative pulses. The thresholds are about 0.5V above and below the reference level.



HP-IL analogue receiver principle



Waveforms of the HP-IL input signal and receiver digital outputs

3.3 HP-IL input signal sampling and frame extraction

Instead of trying to decode the HP-IL frame in real time, the two receiver digital signals are simultaneously sampled at the maximum speed allowed by the uC. A 20 MHz PIC can sample the inputs every 400 ns, which is enough to catch the 1 us pulses.

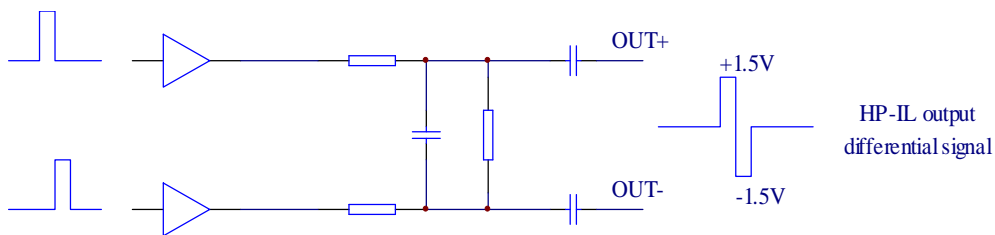
Starting from the first edge, 128 samples are taken for a duration of 51 us, which gives a comfortable 10% margin versus the standard HP-IL frame duration of 46 us.

On the PIC uC, two samples (i.e. 4 bits) are stored in each register in order to fit the full frame into 64 successive registers of a single memory bank.

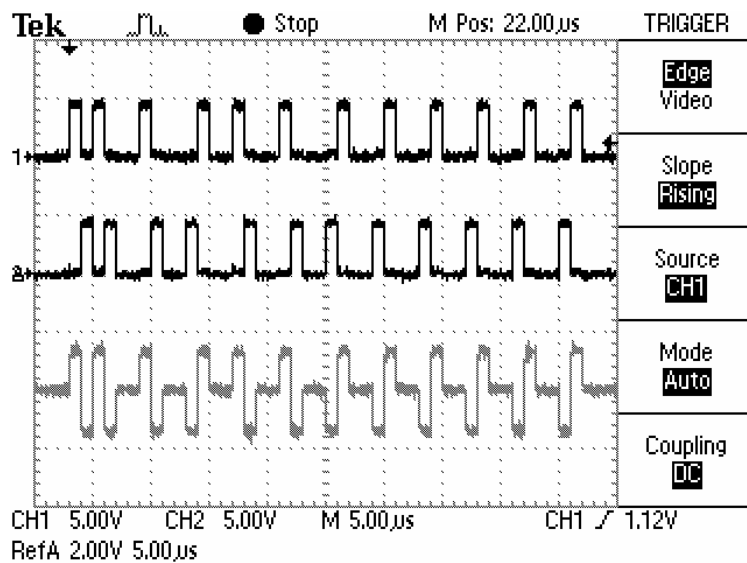
The frame is then extracted from the bit stream by looking at the low and high levels of the input signals and detecting the idle states between the HP-IL bits. This task takes about 500 us on a 20 MHz PIC uC in the current implementation.

3.4 HP-IL transmitter

The output network is used to scale down the output signal to the right level, match the impedance of the HP-IL cables, limit the rise and fall times, and finally block any possible DC part.



HP-IL transmitter principle



Waveforms of the digital transmitter signals and HP-IL output signal

4. HP-IL/serial (TTL level) translator

4.1 General operation

The HP-IL/serial converter translates the HP-IL frames received from the HP-IL input to serial bytes and conversely translates serial bytes received from the serial input to HP-IL frames.

The HP-IL protocol is managed on the computer side to implement the needed functionalities.

The key aspect is that all frames are translated, not only data bytes, and the protocol controller can be either on the HP-IL or computer side.

4.2 Serial link aspects

To transmit an 11-bit HP-IL frame on a standard 8-bit asynchronous serial link, two bytes must be used. One will carry the high part of the frame, the second will carry the low part. A coding scheme has been designed for maximum compatibility with any serial links, and optimum performance.

Two formats are used:

- the first one uses only ASCII 7-bit characters:

001c cebb high byte: higher 5 bits (3 control bits plus data bits 7 and 6)

01bb bbbb low byte: lower 6 data bits

This format is compatible with virtually any serial link and protocol.

- an improved format is using full 8-bit bytes:

001c ccb0 high byte: higher 4 bits (3 control bits plus data bit 7)

1bbb bbbb low byte: lower 7 data bits

The main benefit of this format is that only the low byte is really needed to transmit ASCII data frames (control bits=0, data bit7=0). The choice of using the 8-bit byte format is done by the computer.

To take advantage of the 8-bit format, the protocol has been implemented as follow:

When a frame has to be transmitted to the serial link, the driver will check if the high byte (control bits and data bit 7) is the same than the previously transmitted frame. If yes, it is not transmitted again and only the low byte is sent.

Conversely, if the receiver gets only the low byte, it will use the last received high byte to rebuild the full frame.

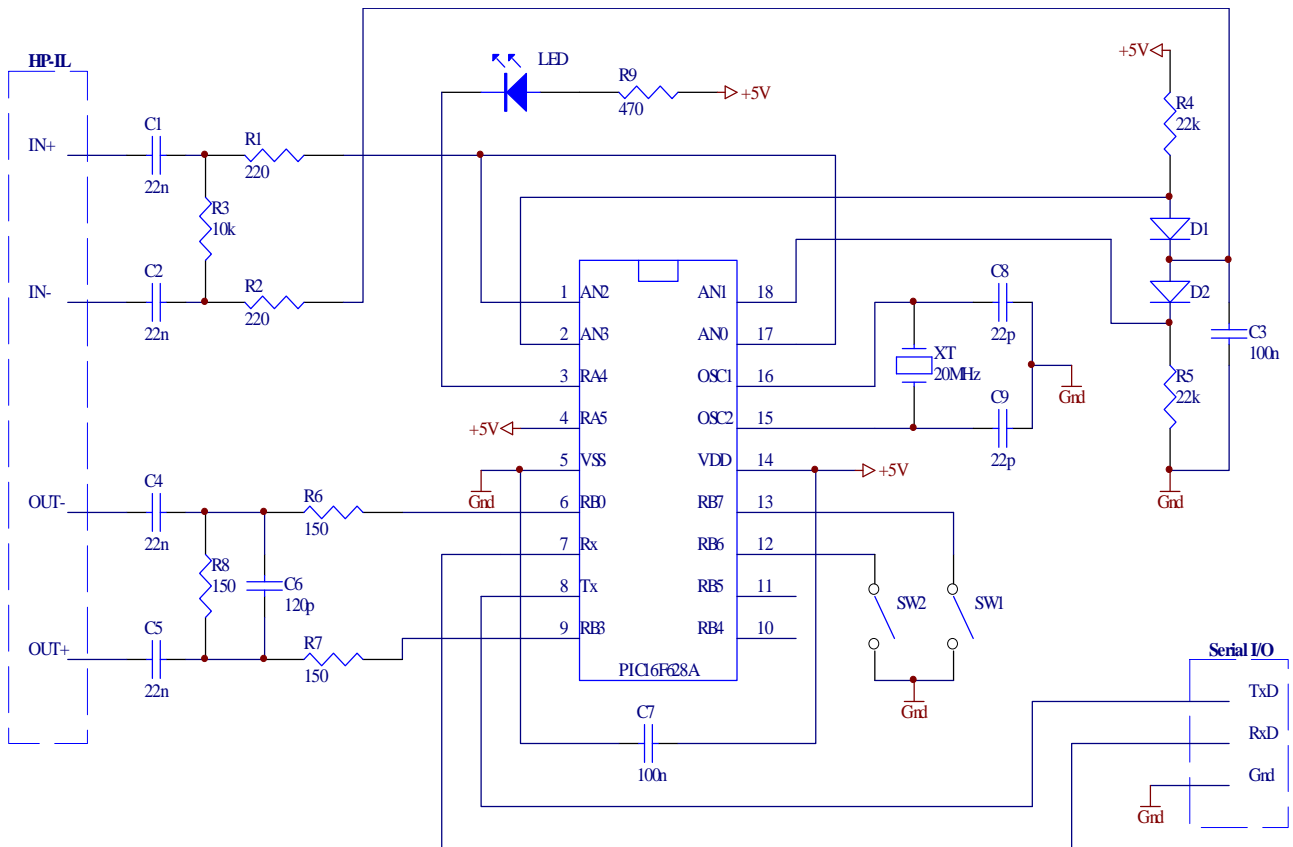
The effect is doubling the effective transfer rate for large text data such as display data or text files. This is specially important for low speed serial link (e.g. 9600 bauds).

4.3 HP-IL protocol considerations

To speed-up the HP-IL operation, a few special processing are done in the HP-IL/serial translator when driven by a controller on the HP-IL side (this is always the case with the HP-41C): IDY frames are locally retransmitted on the HP-IL without transmission to computer on the serial link. RFC frames are managed locally as well. All other frames are sent to the computer side by the serial link for processing, and the returned frame is retransmitted to the HP-IL loop.

Actually, the translator implementation also supports the protocol controller to be on the computer side, such as in the Emu41 or Emu71 applications that can control HP-IL devices on the loop, in this case only the RFC frames are managed locally by the translator and don't have to be explicitly managed on the computer side..

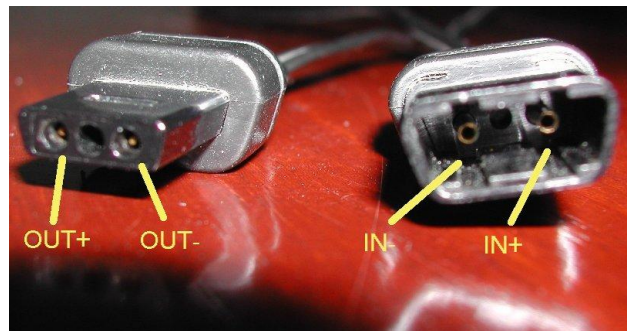
5. HP-IL/serial translator schematic



HP-IL/serial (TTL level) translator schematic

Bill of material:

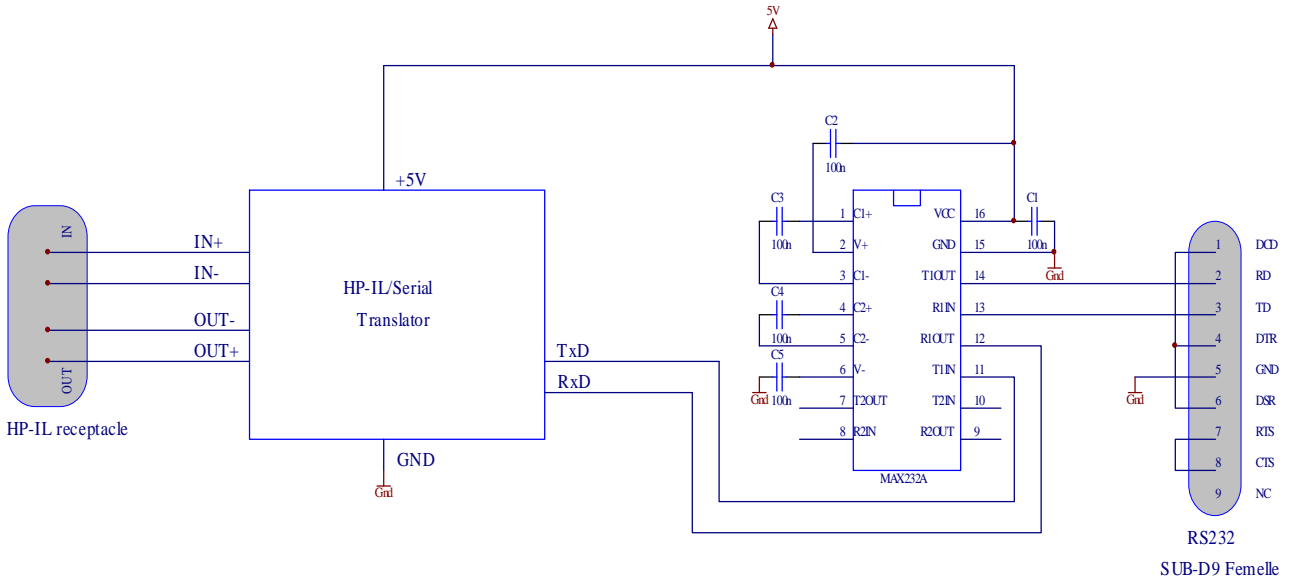
- R1, R2: 220 ohms
- R3: 10 kohms
- R4, R5: 22 kohms
- R6, R7, R8: 150 ohms
- R9: 470 ohms
- C1, C2, C4, C5: 22 nF
- C3, C7: 100 nF
- C6: 120 pF
- C8, C9: 22 pF
- D1, D2: 1N4148
- LED 5 mm, red
- XT 20 MHz
- PIC 16F628A
- One HP-IL cable (cut in 2 halves)



6. Applications

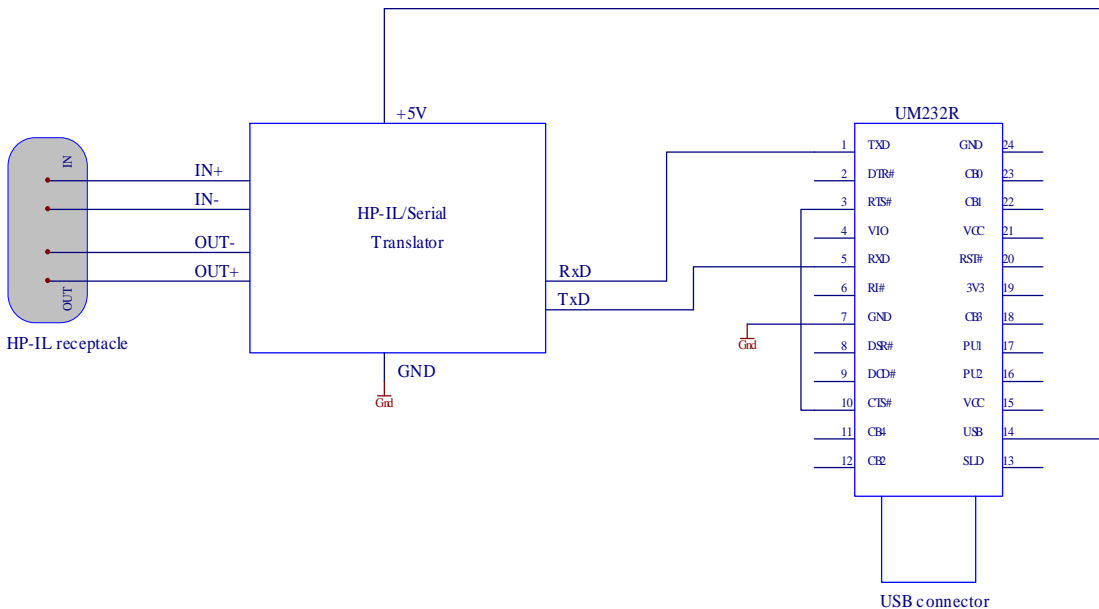
6.1 RS232 and USB PIL-Boxes

A RS232 PIL-Box can be easily built by adding a RS232 level shifter to the HP-IL/serial translator. An external 5V supply is needed.



RS232 PIL-Box

A USB PIL-Box can be built by using a FTDI chip with a minimum of effort and no need to develop special software drivers. The example below uses the UM232R development module from FTDI. The PIL-Box is completely powered by the USB, no external supply is needed.



USB PIL-Box

The PIL-Boxes can be used in place of the classic HP-IL/PC ISA board, provided that the PC software part is adapted to this new link, and add HP-IL capability to virtually any computer.

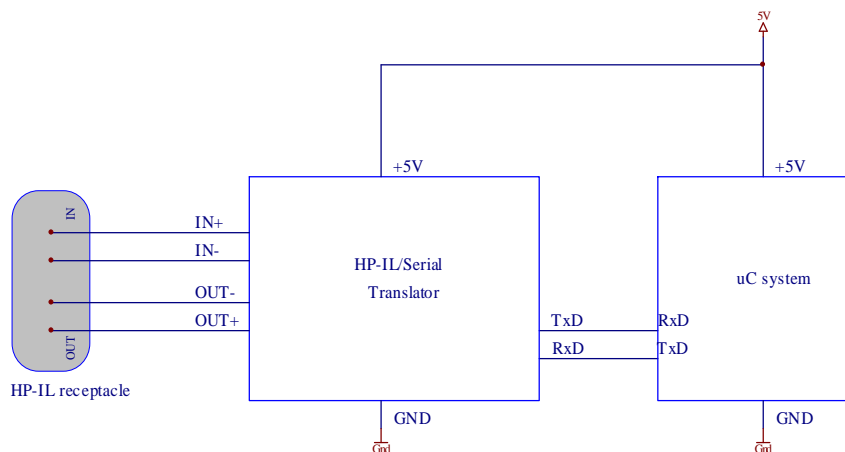
The source code of the implementation of a HP-IL peripheral device emulator (ILPER) on PC using the PIL-Box is freely available. It provides display and mass storage devices to the HP-41C, HP-71B or HP-75C calculator/computers.

The Emu41 and Emu71 PC applications also support the PIL-Box (in both device and loop controller modes) using either a RS232 link or a Virtual Communication Port (VCP) through USB.

6.2 Custom HP-IL devices

New custom HP-IL devices can be built by managing the HP-IL protocol.

It is recommended to use the HP-IL/serial translator as a black box using the TTL level serial lines to communicate with an application processor. High transmission speed, up to 115 kbauds can be used for optimum performance.



Custom HP-IL device

A few application examples:

- HP-IL mass storage device using SD cards,
- HP-IL LCD display unit,
- data acquisition and control systems,
- various HP-IL interfaces (I2C, SPI,...),
- new calculator with HP-IL capability !
- etc...

7. Final notes

This implementation has the following deviations vs the HP specification:

- It is probably less robust than the HP implementation, but still very acceptable for education, research or hobby activities which is the aim of this work.
- Although the HP-IL lines are AC coupled, this implementation does not provide true galvanic insulation on the PIL-Box side. The galvanic insulation is ensured by the other side (the HP-IL module for instance).
- The HP-IL lines are not balanced like in the pulse transformer implementation, they carry some common mode voltage and are more susceptible to generate EMI. A simple ferrite chock can improve this point, if really needed.
- The HP-IL frame decoding is quite simple and may be improved by a more elaborated decoding and checking logic (in the software part), for instance checking the synchronisation bit or checking each bit is made of one positive and one negative pulse. However, the logic has been found good enough to reject common parasitic spikes, by just checking that exactly 11 bits are decoded in each frame.
- The theoretical maximum transfer rate is slower than when using the 1LB3 HP-IL chip, the software decoding of the incoming frames takes 500 us and sets a limit to the maximum data rate at 2 kbytes/second. This is not a limitation with the HP-41C which is actually much slower, and may be noticeable with the HP-71B when using high serial speed (115 kbauds).

ESD aspects:

Serial resistors have been used on each PIC input connected to HP-IL lines, this should be enough to withstand usual ESD events in conjunction to the PIC built-in protection. Additional ESD protection can be added if needed.

This project aims for education, research or hobby activities, and should not be used for industrial or professional applications.

Permission is given to use the HP-IL/serial translator description for personal use, but no commercial usage is allowed without written permission of the author.